Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 3-37 are pending in the application, with Claims 3, 14, 16, 32, and 35 being the independent claims. Claims 1, 14, and 35 are sought to be amended. Claims 14 and 35 are amended only to correct for typographical errors, and the scope of claims 14 and 35 remains unchanged. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

Claims 3-37 stand rejected under 35 U.S.C. 102(e) as being allegedly unpatentable over U.S. Pat. No. 6,216,252 issued to Dangelo *et al.* ("Dangelo"). Applicant respectfully traverses.

Regarding claim 3, Applicant respectfully submits that Dangelo does not teach each and every element of claim 3. For example, Dangelo neither teaches nor suggests a method for predicting the physical characteristics of an electronic design before gate-level implementation. Instead, Dangelo's method provides physical characteristic data through multiple simulations of the gate-level implementation. As stated in Dangelo, col. 4, lines 36-37, "the gate-level design description is simulated."

The Examiner alleges that "the prior art of Dangelo teaches wire delay estimation information for placement of buffers for optimizing logic block design in column 14, line

56 through column 15, line 7 where wire delay information module is performed using the specified requirement of timing characteristics," and that this information meets the claimed features. *See*, Office Action, section 3, page 4. Applicants respectfully disagree.

Placement based information, as described in the specification, includes actual measurements taken from a variety of placed-and-routed physical implementations of each logic structure. These measurements are taken prior to any logic synthesis, and are stored within the logic building blocks ("LBBs") in the LBB library. As stated in para. 0079 of the specification, "in the characterization process, logical and physical implementations of each LBB are built and characterized by varying some or all, individually or in combination, of the following input parameters that affect the area and speed of a LBB physical implementation." Since the information is based on previously placed and routed implementations, it is "placement based information." Because of these previous measurements, information about timing, load, etc., can be calculated without detailed or physical placement and routing of the particular circuit design involved.

Dangelo, on the other hand, estimates new information for optimizing each circuit design, as shown in col. 14, lines 56-57: "A Block Level Delay Estimator 808 provides the optimization tool with pessimistic wire delays." The Examiner refers to col. 8, lines 41-53 of Dangelo for support of his rejection. However, Applicant respectfully submits that this section of Dangelo does not discuss using placement based information to optimize the design. Indeed, the cited section states the opposite, that "typically, decisions concerning the selection and placement of modules is deferred." Although Dangelo discusses, in the next paragraph, estimating physical parameters, it does not

teach or suggest using placement based information to optimize logic building blocks as recited in claim 3. Therefore, Dangelo neither teaches nor suggests optimizing a network of technology-independent LBBs logically and physically using placement based information, as recited in claim 3.

Additionally, because Dangelo provides physical data through multiple simulations of a gate-level implementation, Dangelo optimizes at the gate level. Indeed, as stated in Dangelo, optimization is performed "on individual or small clusters of gates." *See*, Dangelo, col. 10, line 67 - col. 11, line 3. Thus, optimization does not occur on a network of technology-independent logic building blocks as recited in claim 3. As discussed in paragraph 0020 of the present application, "the use of LBBs elevates the pre-characterized library approach from the conventional gate level to a complex-structure module level."

The specification further details the difference between logic structures and implemented gates. As discussed in paragraph 0020 of the present application, the phrase "logic building blocks" as used in the present application describe "a high level, *technology-independent* description of a logic structure that has performance data fully characterizing its performance envelope over a range of different physical implementations." In addition, "a single logic building block may contain the equivalent of several hundred gates." *See*, specification, para. 0094.

The only blocks discussed in Dangelo are "mega-cells". However, the mega-cells of Dangelo are not technology independent and do not perform the same function as the logic building blocks of the present application. As stated in Dangelo, the mega-cells "are generally developed beforehand" and "no optimization is required on these blocks." *See*, Dangelo, col. 12, lines 40-55. Additionally, "mega-cells are static and do not

change from one design to the other." Id., col 15, lines 60-62. Because the mega-cells in Dangelo are fixed and are not optimized, they cannot be altered to work with various technologies. Thus, they are not technology independent as claimed in claim 3. Further, since they are fixed, the mega-cells' physical characteristics cannot change and placement-based information would not affect the physical characteristics of the mega-cells.

For at least these reasons, Applicant respectfully submits that claim 3 is patentable over Dangelo. Reconsideration and withdrawal of the rejection of claim 3 is respectfully requested.

Regarding claims 4-13, the Examiner contends that the subject matter of these claims are well known. Applicant disagrees. For example, as the concepts of using placement based information and logic building blocks were pioneered by the Applicant, they could not have been well-known at the time of invention as suggested by the Examiner. Further, the Examiner is respectfully reminded that "assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must always be supported by citation to some reference work" and "it is never appropriate to rely solely on 'common knowledge' in the art without evidentiary support in the record." *See*, MPEP § 2144.03. Thus, Applicant respectfully requests that the Examiner provide references showing the features of claims 4-13 in accordance with MPEP § 2144.03, or that the rejection of claims 4-13 be withdrawn.

Regarding claim 14, the Examiner's rejection of claim 14 does not take into consideration a previous amendment to claim 14. Specifically, the Examiner does not address or provide evidence for any teaching in Dangelo that describes creating a virtual prototype using placement based information. For the same reasons as discussed with

respect to claim 3, Applicant submits that Dangelo neither teaches nor suggests using placement based information. Thus, Dangelo also does not teach or suggest virtual prototyping using placement based information. For at least these reasons, Applicant respectfully submits that claim 14 is patentable over Dangelo. Reconsideration and withdrawal of the rejection of claim 14 is respectfully requested.

Regarding claim 15, Applicant respectfully disagrees with the Examiner's unsupported contention that the subject matter is well known in the art. Applicant kindly requests that the Examiner provide a reference showing this feature in accordance with MPEP § 2144.03, or that the rejection of claim 15 be withdrawn.

Regarding claim 16, Applicant reiterates the discussion of claim 3 regarding logic building blocks. Specifically, since Dangelo does not disclose logic building blocks in the context of the present application, Dangelo neither teaches nor suggests mapping the model into logic building blocks as claimed in claim 16. The Examiner references col. 8, lines 41-43, col. 9, lines 1-8, and Fig. 4 of Dangelo in support of his rejection. However, Applicant respectfully submits that these sections of Dangelo neither teach nor suggest logic building blocks having a logic structure including a plurality of gates as claimed in claim 16.

Further, Dangelo neither teaches nor suggests "each logic block having performance data based on placed and routed implementations of that logic building block," as recited in claim 16. As discussed with respect to claim 3, Dangelo does not teach or suggest using data from previously placed and routed implementations of each block. For example, Dangelo optimizes based on estimates rather than data from placed and routed implementations.

For at least these reasons, Applicant respectfully submits that claim 16 is patentable over Dangelo. Reconsideration and withdrawal of the rejection of claim 16 is respectfully requested.

Regarding claims 17-30, Applicant respectfully disagrees with the Examiner's unsupported contention that the subject matters of these claims are well known in the art. Applicant kindly requests that the Examiner provide references showing these features in accordance with MPEP § 2144.03, or that the rejections of claims 17-30 be withdrawn.

Regarding claim 31, Applicant respectfully submits that claim 31 is patentable over Dangelo for at least the reasons as discussed with respect to claim 16, as claim 31 depends from claim 16. Reconsideration and withdrawal of the rejection of claim 31 is respectfully requested.

Regarding claim 32, Applicant respectfully submits that Dangelo neither teaches nor suggests "creating physical implementations of a logic building block" and "monitoring area and placement based performance data of each physical implementation" as claimed in claim 32. Any performance data described in Dangelo, such as described with respect to the delay back annotation (*See*, Dangelo, col. 11, lines 57-64) is only estimated data; it is not placement based data as described with respect to claim 3. The Examiner points to col. 1, lines 61-67 and col. 3, lines 48-55 of Dangelo in support of the rejection. Applicant respectfully submits that neither of these sections teaches nor suggests monitoring, much less monitoring area and performance data of each physical implementation.

Additionally, since, Dangelo outputs a gate level design ("in a 'physical simulation' step, the gate-level design description is simulated", col. 4, lines 36-37), the physical implementation is also at the gate level. Thus, the physical implementation is

not at the level of a logic building block having "a higher level of abstraction than gates" as claimed in claim 32.

For at least these reasons, Applicant respectfully submits that claim 32 is patentable over Dangelo. Reconsideration and withdrawal of the rejection of claim 32 is respectfully requested.

Regarding claims 33-34, Applicant respectfully disagrees with the Examiner's unsupported contention that the subject matters of these claims are well known in the art. Applicant kindly requests that the Examiner provide references showing these features in accordance with MPEP § 2144.03, or that the rejections of claims 33-34 be withdrawn.

Regarding claim 35, Applicant respectfully submits that Dangelo does not teach or suggest each and every element of claim 35. For example, for the same reasons discussed with respect to claim 16, Dangelo does not teach or suggest logic structures "having performance data based on placed and routed implementations of that logic structure" as recited in claim 35. Dangelo only discusses placement and routing data in the context of gate level implementation. Specifically, "the delays can be back annotated to be used by the gate level Optimizer." *See*, Dangelo, col. 11, lines 62-64. Thus, Applicant respectfully submits that claim 35 is patentable over Dangelo. Reconsideration and withdrawal of the rejection of claim 35 is respectfully requested.

Regarding claims 36-37, Applicant respectfully disagree with the Examiner's unsupported contention that the subject matters of these claims are well known in the art. Applicant kindly requests that the Examiner provide references showing these features in accordance with MPEP § 2144.03, or that the rejections of claims 36-37 be withdrawn.

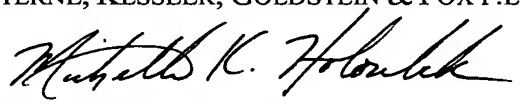
Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



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